ABSTRACT OF THE DISCLOSURE

CMOS device arrangements have a surface channel, and a method for manufacturing the same by forming a multi-layer that includes a first metal layer, a polysilicon layer and a second metal layer having a work function from 4.8 through 5.0eV on a cell region NMOS and a gate electrode of a peripheral circuit region PMOS, and by forming a multi-layer that includes a polysilicon layer and a second metal layer on a gate electrode of a peripheral circuit region NMOS. Because of the multi-layered gate electrode, a separate transient ion implantation process is not necessary, which consequently simplified the CMOS manufacturing process, while maintaining the threshold voltage of each peripheral circuit region – 0.5V and below, and the threshold voltage of the peripheral circuit region NMOS +0.5V and below. Meantime, since the cell NMOS has the threshold voltage of +1V thanks to the first metal layer, no separate back bias is necessary, thereby forming a device with low power consumption, which consequently improves characteristics, yield and reliability of the device.